A Curvature Compensation Technique for Bandgap Voltage References Using Adaptive Reference Temperature

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Abstract – A curvature compensation technique for bandgap voltage references that utilizes an adaptive reference temperature is presented. This compensation technique is intended for high-resolution temperature-stable analog-digital converters. A test circuit had been designed in a 0.6 *m*m CMOS technology to implement this technique. The reference voltage has a simulated temperature coefficient of 2.3 ppm/°C over the temperature range of –40 to 90 °C.

I. INTRODUCTION

Voltage reference circuits are widely used l in data converters. Bandgap voltage references (BVR) have become the most popular solution since they were first introduced in the 80's. However, even the BVR have performance limitations due to the nonlinear temperature variation of its output voltage. The temperature variation of the BVR output voltage is illustrated in Fig. 1 where the deviation in output voltage due to the "curvature" over the temperature range from 20C to 100C is typically around 35 ppm even for a basic well-designed reference. This deviation is too large for many applications. Several approaches [3], [5], [6] have been proposed to correct the curvature of the BVR output voltage (V_{REF}). The proposed solutions attempt to cancel the nonlinear components of V_{REF} using continuous and differentiable higher-order temperature terms. These correction terms are either difficult to generate or unsuitable for standard CMOS process [3],[6]. Moreover, these solution are sensitive to process variations because of the need to closely match the nonlinear coefficients of opposite signs in order to have decent cancellation [5],[6]. In this paper, a curvature compensation alternative that does not utilize continuous and differential nonlinear cancellation is presented.

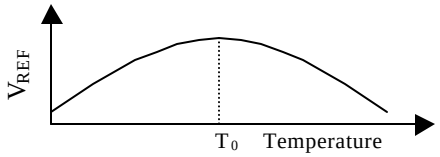

Fig. 1 Temperature variation of BVR output voltage

II. BANDGAP VOLTAGE REFERENCE

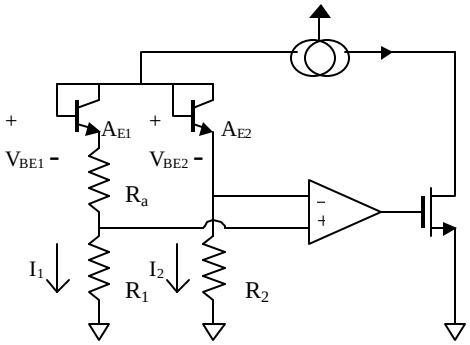

Fig. 2 Two diodes that generate V_{BE} and PTAT voltage

Fig. 2 shows a standard BVR circuit with two diode-connected BJTs, which have a base-emitter area ratio of A_{E1}/A_{E2}. The closed-loop op amp forces the same voltage drop across R_1 and R_2. The temperature characteristic of V_{BE} is governed by the following expression [2],[4]:

$$V_{BE}(T) = V_{G0}\left(1-\frac{T}{T_0}\right)+\left(\frac{T}{T_0}\right)V_{BE0} - \eta\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_0}\right)+\left(\frac{kT}{q}\right)\ln\left(\frac{J_C}{J_{C0}}\right) \qquad (1)$$

where V_{G0} is the silicon bandgap voltage extrapolated to 0 °K (~1.206V), k is the Boltzmann's constant, η is a process dependent constant,T_0 denotes the reference

temperature, V_{BE0} is the base-emitter voltage drop at the reference temperature and J_{C0} is the collector current density evaluated at the reference temperature T_0. A PTAT voltage (proportional to absolute temperature) can be derived from the difference between the V_{BE} drops of two transistors. If follows from (1) that:

$$V_{PTAT} = \Delta V_{BE} = V_{BE2} - V_{BE1} \quad (2)$$

where

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{A_{E1}}{A_{E2}} \cdot \frac{I_2}{I_1}\right) \quad (3)$$

In (3), the collector current density J_C has been replaced by $J_C=I/A_E$ where A_E is the effective base-emitter area. V_{REF} is then obtained by adding the PTAT voltage (ΔV_{BE}) to the "inversely" PTAT voltage (V_{BE}), which yields the following expression:

$$V_{REF} = V_{BE} + K \cdot \Delta V_{BE} \quad (4)$$

K is chosen to cancel the first order temperature variation of V_{BE}. In the implementation of this paper, a switched-capacitor circuit as depicted in Fig. 3 was used to perform the weighted addition of (4).

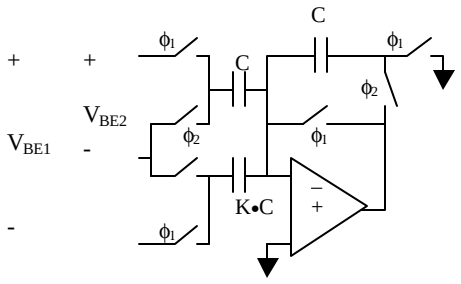

Fig. 4 Switched-capacitor circuit that performs weighted addition

If it is assumed that $J_C/J_{C0}=T/T_0$ [2] and that value of K is chosen to cancel the first-order temperature, (4) can be expanded and rewritten as [2]:

$$V_{REF} = V_{G0} + (\eta - 1)\frac{kT}{q}\left[1 + \ln\left(\frac{T_0}{T}\right)\right] \quad (5)$$

The second term in (5) is the nonlinear component of V_{REF}. To examine the temperature variation of V_{REF}, the expression for $\partial V_{REF}/\partial T$ is derived [2]:

$$\frac{\partial V_{REF}}{\partial T} = (\eta - 1)\frac{k}{q} \ln\left(\frac{T_0}{T}\right) \quad (6)$$

As (6) describes, V_{REF} has zero temperature variation ($\partial V_{REF}/\partial T=0$) at $T=T_0$ and V_{REF} has minimal variation with temperature for T around T_0. Therefore, if a BVR circuit has an adaptive T_0 that varies over temperature, then a V_{REF} with a minimal temperature variation over a wide temperature range can be realizable.

III. CURVATURE COMPENSATION

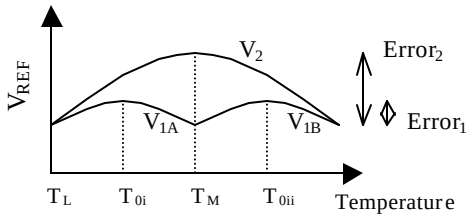

Fig. 4 BVR circuit with adaptive T_0

The assumed relationship of $J_C/J_{C0}=T/T_0$ [2] can be readily realized at the circuit level. This relationship suggests that T_0 is adjustable through changing the DC bias current of the BVR circuit. Assume that the circuit in Fig. 2 is designed to operate with a reference temperature at T_{0i} when the temperature range is between T_L and T_M as illustrated in Fig. 4. When the temperature range gets above T_M, the BVR circuit will be calibrated such that it will now operate with a reference temperature at T_{0ii}. Overall, the BVR with adaptive T_0 has a two-segment V_{REF} curve designated by V_{1A} and V_{1B} in Fig. 4. With the segmented correction, the maximum error caused by the curvature is $Error_1$. This can be contrasted to the conventional BVR that is referenced to temperature T_M and has the V_{REF} curve of V_2 as depicted in Fig. 4 with a maximum error of $Error_2$. This illustration demonstrates that the adaptive T_0 BVR compensation technique significantly improves the V_{REF} accuracy over

a wide temperature range. To further improve the V_{REF} accuracy, the overall temperature range can be partitioned into additional regions each of which spans a correspondingly smaller temperature range. In this work, the temperature range was partitioned into four regions (quadrants). To address these four regions, an ADC needs to perform a two-bit temperature-digital signal conversion. The region selection has been implemented in a two-step process. In the first step, an uncalibrated BVR is used to generate the reference voltage of the ADC that is used to sense temperature. The digital signal is then fed to the BVR to select the proper quadrant as interpreted by the 2 bit digital signal. With the BVR compensated, the ADC is now ready for doing data conversion. The system block diagram is shown in Fig. 5.

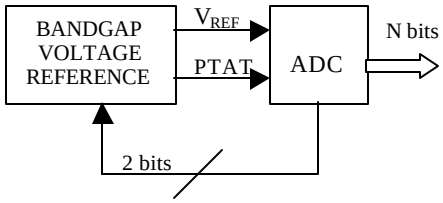

Fig. 5 System block diagram for BVR curvature compensation

IV. CIRCUIT IMPLEMENTATION

Consider the circuit in Fig. 6, which is a slight modification from the circuit in Fig. 2. The switches S_0 to S_3 are controlled by the 2 bits digital signal that assigns the appropriate temperature quadrant. The resistances R_{10}, R_{11}, R_{12} and R_{13} are sized such that $R_{10}<R_{11}<R_{12}<R_{13}$. Calibration is implemented by selecting the appropriate resistor to adjust the current in the left-most transistor of Fig. 6. As indicated by the relationship $J_C/J_{C0}=T/T_0$, adjusting J_C results in a change of T_0 is mentioned. Although adjusting J_C accomplishes the desired goal of moving T_0 along the horizontal axis, it can be shown that the magnitude of the peak value of V_{REF} in any quadrant is also affected by J_C. If the temperature is in the first quadrant, then S_0 is closed and the circuit has a reference temperature at T_{01} as depicted by the segment labeled V_{REF1} in Fig. 7a. Likewise, if the temperature is in the second quadrant, S_0 is open and S_1 is closed to increase the effective resistance R_1. This action has the net effect of increasing the current flowing through the BJT pair. By doing so, the reference temperature of the BVR circuit is shifted from T_{01} to T_{02} and so on. In order to align the peak values of the four V_{REF} curves of different T_0 to realize a flat V_{REF}, DC level adjustment is required, as indicated in Fig. 7b. This is realized through sizing the feedback capacitor dynamically in the switched-capacitor circuit depicted in Fig. 3.

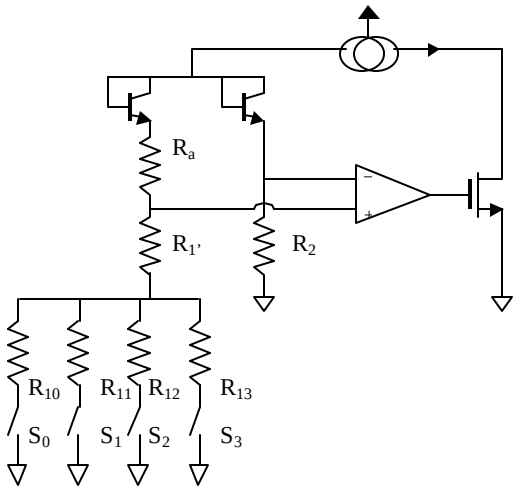

Fig. 6 Modified BVR circuit that implements adaptive T_0 compensation technique

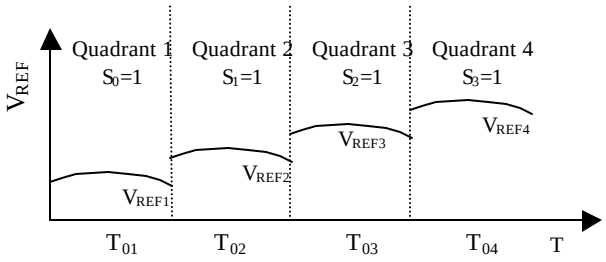

Fig. 7a V_{REF} measured from the circuit in Fig. 5

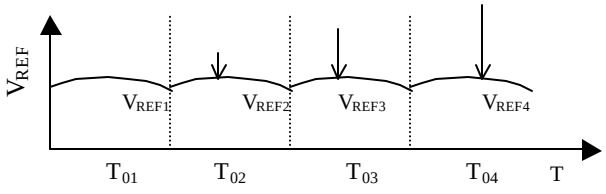

Fig. 7b Flat V_{REF} is realized after DC level adjustment

V. RESULT

The circuit has been designed, laid-out and is currently awaiting fabrication. The output of the voltage reference, $V_{REF,}$ has been simulated in HSPICE. Simulation results of the circuit extracted from the layout predict a temperature coefficient of at most 2.3 ppm/°C over the temperature range of –40 to 90 °C. The simulated V_{REF} varies between 1.2166V to 1.2169V. The chip occupies an area of 0.39 mm^2, and consumes 0.756mW at 90 °C and 0.468mW at –40 °C with a single supply voltage of V_{DD} =3V.

VI. DISCUSSION

The proposed BVR circuit is affected by other non-idealities, specifically the offset voltage of the op amp and process parameter variations. The offset voltage causes the voltage drops across R_1 and R_2 to be different. The error caused by the offset voltage of the op amp has been compensated with a chopper technique [1]. Process variations such as sheet resistance deviation and process corner differences can move the reference temperature in each temperature quadrant away from the quadrant center causing the curvature error to increase. To counteract this affect, R_a and R_2 are trimmed using switches similar to those depicted in Fig. 6 to center the reference temperature in each temperature quadrant.

VII. CONCLUSION

A BVR curvature compensation scheme using an adaptive reference temperature circuit has been presented. This technique is easy to implement and trim in contrast to conventional continuous and differentiable curvature compensation techniques.

REFERENCES

[1] A. Bakker, J. Huijsing, *High-Accuracy CMOS Smart Temperature Sensors*, Kluwer Academic, 2000.

[2] D.A. Johns, K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 1997.

[3] M. Gunawan, G.C.M. Meijer, J. Fonderie, and J.H. Huijsing, "A curvature-corrected low-voltage bandgap reference," *IEEE Journal of Solid State Circuits*, vol.28, no.6, pp.667-670, June 1993.

[4] Y.P. Tsividis, "Accurate analysis of temperature effects in IC-VBE characteristics with application to bandgap reference sources." *IEEE Journal of Solid-State Circuits*, vol.sc-15, no.6, pp. 1076-1084, Dec. 1980.

[5] M.A.P. Pertijs, A. Bakker, J.H. Huijsing, "A high-accuracy temperature sensor with second-order curvature correction and digital bus interface." *ISCAS 2001*, vol.1, pp. 368 –371, 2001

[6] I.M. Filanovsky, Y.F. Chan, "BICMOS cascaded bandgap voltage reference," *IEEE 39th Midwest symposium on Circuits and Systems*, vol.2, pp. 943 –946, 1996